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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,083	11/15/2003	Ari Aviram		9492

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EXAMINER

COLEMAN, WILLIAM D

ART UNIT PAPER NUMBER

2823

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/714,083	<b>Applicant(s)</b> AVIRAM, ARI	
	<b>Examiner</b> W. David Coleman	<b>Art Unit</b> 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 11 November 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on November 15, 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

# DETAILED ACTION

## *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

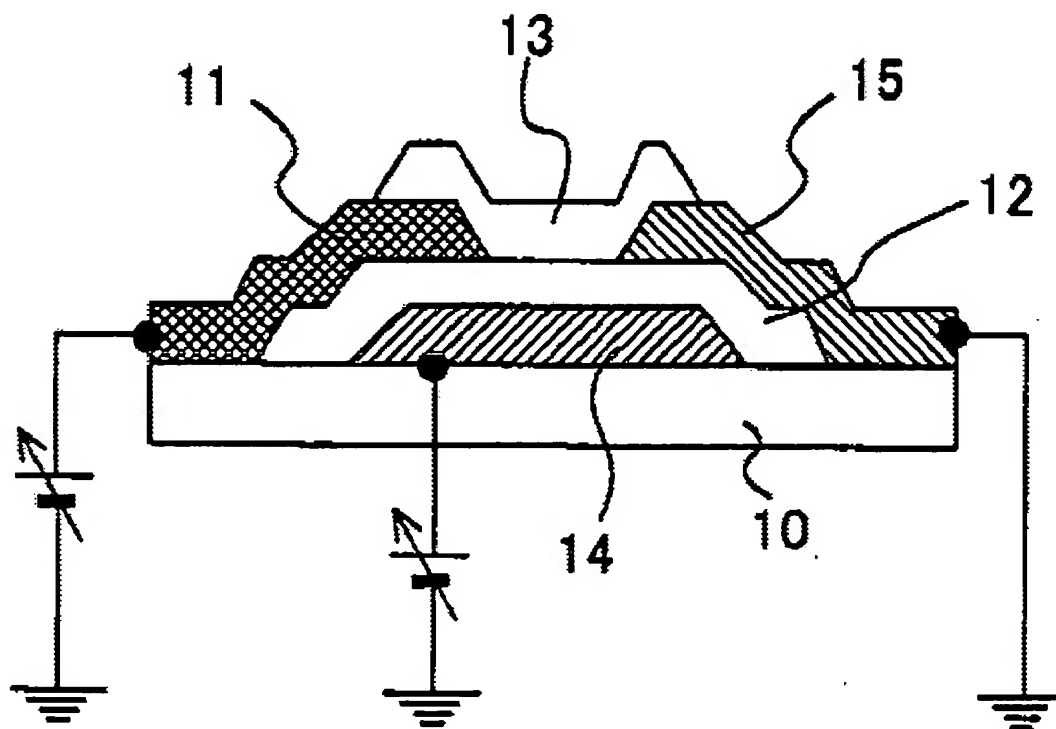
A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanabe et al.,

U.S. Patent Application Publication Number 2004/0012018 A1.

3. Tanabe discloses a semiconductor process as claimed. See **FIGS. 1-8**, where Tanabe teaches the claimed limitations.



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4. Pertaining to claim 1, Tanabe teaches a method of fabrication of electrical contacts for molecular electronic transistors, comprising the steps of:

wiring a three-terminal molecule or an aggregate thereof to serve as an electronic transistor, the electronic transistor comprising a gate electrode 14, a source electrode 11, and a drain electrode 15,

wherein the source electrode and the drain electrode are fabricated from a first previously-determined metal (platinum, palladium, chromium) and the gate electrode is fabricated from a second previously-determined metal (aluminum, copper, nickel, chromium or an alloy thereof), functioning to allow for simultaneous attachment of molecules to the source electrode, drain electrode, and gate electrode in a previously-determined order, for the creation enhanced integrated circuits.

5. Pertaining to claim 2, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 1, wherein the method is utilized in conjunction with mixed-valence transistors (Tanabe teaches forming both n-type and p-type transistors).

6. Pertaining to claim 3, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 2, wherein the method utilizes a chemical means (CVD, chemical vapor deposition is a chemical means).

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7. Pertaining to claim 4, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 2, wherein the method utilizes a photochemical means (the Examiner takes the position that it is well known to use photoresist in the semiconductor fabrication technology and that photoresist is a photochemical means).

8. Pertaining to claim 5, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 2, wherein the method utilizes an electrochemical means (see [0023]).

9. Pertaining to claim 6, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 1, wherein the electrode is of a material selected from the group consisting of platinum, gold, or other previously-determined metal.

10. Pertaining to claim 7, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 1, wherein the method is utilized in conjunction with the source electrode, drain electrode, and gate electrode existing in one plane (when viewing from a top view the electrodes are all in the same plane).

11. Pertaining to claim 8, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 1, wherein the method is utilized in conjunction with two electrodes in one plane, and a third electrode in plane perpendicular thereto.

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12. Pertaining to claim 9, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 8, wherein the method is utilized in conjunction with the source electrode and drain electrode in one plane, and the gate electrode in a plane perpendicular thereto.

13. Pertaining to claim 10, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 9, wherein molecules comprise specific alligator clips on source and drain terminals which can connect to a first metal, and further comprise a distinct alligator clip on a gate terminal which binds exclusively to a second metal.

14. Pertaining to claim 11, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 10, wherein the molecules are attached to the source electrode, drain electrode, and gate electrode by self-assembly as neutral species.

15. Pertaining to claim 12, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 10, wherein the molecules are attached to the source electrode, drain electrode, and gate electrode by self-assembly as charged species.

16. Pertaining to claim 13, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 1, wherein the gate electrode is of a material selected from the group consisting of titanium, chrome, nickel, polysilicon, silicon, aluminum, tin oxide indium, tin oxide, and gallium arsenide.

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17. Pertaining to claim 14, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 1, wherein the source electrode is of a material selected from the group consisting of platinum, rhodium, silver, gold, and copper.

18. Pertaining to claim 15, Tanabe teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 1, wherein the drain electrode is of a material selected from the group consisting of platinum, rhodium, silver, gold, and copper.

19. Claims 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelley et al., U.S. Patent 6,433,359 B1.

20. Kelley discloses a semiconductor process as claimed. See **FIGS. 1-3**, where Kelley teaches the claimed limitations.

21. Pertaining to claim 16, Kelley teaches a method of fabrication of electrical contacts for molecular electronic transistors wherein:  
a molecule is wired as a transistor by distinguishing between a source / drain metallurgy and a gate metallurgy, and by providing previously-determined alligator clips which function to direct the molecule toward a proper connection,  
wherein the alligator clips on the source / drain chain are -SH groups, and the alligator clip on the gate chain is a phosphate group,  
a metal-electrode pattern is provided on an insulating surface with gaps in previously determined locations in which molecules belong,  
wherein the size of each gap is tailored to fit a length of the molecule,

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wherein the gate electrode is fabricated from aluminum, which couples specifically to the phosphate alligator clip on the molecule (gate chain), and the source / drain electrodes are fabricated from platinum, which couples to the -SH alligator clips on the corresponding chain, a surface containing the electrode pattern then immersed in a solution containing the molecules, functioning to allow self-assembly to occur spontaneously.

22. Pertaining to claim 17, Kelley teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 16, wherein a molecule is prepared in a doubly-oxidized state, with two electrons missing, and the electrochemistry step is that of reduction;

as a negative voltage is applied.

23. Pertaining to claim 18, Kelley teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 16, wherein the method utilizes photochemical oxidation, and the chip is immersed in a concentrated solution containing molecules, followed by rinsing, and the circuit is immersed in carbon tetrachloride and irradiated with UV radiation to form a mixed-valence state (see example 1).

24. Pertaining to claim 19, Kelley teaches the method of fabrication of electrical contacts for molecular electronic transistors as described in claim 16, the molecule is provided with two -SH terminal groups functioning as alligator clips, an electrode pattern is provided on an insulating surface with gaps in locations where the molecules belong, the source / drain electrodes are



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fabricated from gold, the gate electrodes are fabricated from aluminum, the surface containing the electrode pattern is immersed in a solution containing the molecules, functioning to allow self-assembly to occur spontaneously.

### ***Information Disclosure Statement***

25. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

### ***Drawings***

26. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the electrode connections which are supposedly all in one plane must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

27. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

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must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Conclusion*

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'W. David Coleman'.

W. David Coleman  
Primary Examiner  
Art Unit 2823

WDC